

Small Signal MOSFET

60 V, 380 mA, Single, N-Channel, SOT-23

2N7002K, 2V7002K

Features

- ESD Protected
- Low R_{DS(on)}
- Surface Mount Package
- 2V Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Low Side Load Switch
- Level Shift Circuits
- DC-DC Converter
- Portable Applications i.e. DSC, PDA, Cell Phone, etc.

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

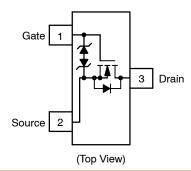
Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	V
Gate-to-Source Voltage	V _{GS}	±20	V
	Ι _D	380 270	mA
	Ι _D	320 230	mA
Power Dissipation Steady State 1 sq in Pad Steady State Minimum Pad	P _D	420 300	mW
Pulsed Drain Current (t _p = 10 μs)	I _{DM}	5.0	Α
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C
Source Current (Body Diode)	I _S	300	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Surface-mounted on FR4 board using 1 sq in pad size with 1 oz Cu.
 Surface-mounted on FR4 board using 0.08 sq in pad size with 1 oz Cu.

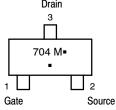
V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
60 V	1.6 Ω @ 10 V	380 mA
	2.5 Ω @ 4.5 V	300 IIIA

SIMPLIFIED SCHEMATIC



MARKING DIAGRAM **& PIN ASSIGNMENT** Drain

SOT-23 **CASE 318** STYLE 21



= Specific Device Code* 704 M = Date Code* = Pb-Free Package

(Note: Microdot may be in either location) *Specific Device Code, Date Code or overbar orientation and/or location may vary depending upon manufacturing location. This is a representation only and actual devices may not match this drawing exactly.

ORDERING INFORMATION

Device	Package	Shipping [†]
2N7002KT1G, 2V7002KT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
2N7002KT7G	SOT-23 (Pb-Free)	3500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	300	°C/W
Junction-to-Ambient - t ≤ 5 s (Note 3)		92	
Junction-to-Ambient - Steady State (Note 4)		417	
Junction-to-Ambient - t ≤ 5 s (Note 4)		154	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	-	•		-			-
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				71		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			1	μΑ
		V _{DS} = 60 V	T _J = 125°C			10	
		V _{GS} = 0 V, V _{DS} = 50 V	T _J = 25°C			100	nA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V	/ _{GS} = ±20 V			±10	μΑ
		V _{DS} = 0 V, V	/ _{GS} = ±10 V			450	nA
		V _{DS} = 0 V, \	/ _{GS} = ±5.0 V			150	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 250 \mu A$		1.0		2.3	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				4.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$ $V_{GS} = 4.5 \text{ V}, I_D = 200 \text{ mA}$			1.19	1.6	Ω
					1.33	2.5	
Forward Transconductance	9FS	$V_{DS} = 5 \text{ V}, I_{D} = 200 \text{ mA}$			530		mS
CHARGES AND CAPACITANCES							
Input Capacitance	C _{ISS}				24.5	45	pF
Output Capacitance	C _{OSS}	G.5	f = 1 MHz, = 20 V		4.2	8.0	
Reverse Transfer Capacitance	C _{RSS}	•DS ·	- 20 V		2.2	5.0	
Total Gate Charge	Q _{G(TOT)}				0.7		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V	, V _{DS} = 10 V;		0.1		
Gate-to-Source Charge	Q_{GS}	I _D = 2	00 mA		0.3		
Gate-to-Drain Charge	Q_{GD}	1			0.1		
SWITCHING CHARACTERISTICS, V_{GS}	= V (Note 6)						
Turn-On Delay Time	t _{d(ON)}				12.2		ns
Rise Time	t _r	V_{GS} = 10 V, V_{DD} = 25 V, I_{D} = 500 mA, R_{G} = 25 Ω			9.0		
Turn-Off Delay Time	t _{d(OFF)}				55.8		
Fall Time	t _f				29		
DRAIN-SOURCE DIODE CHARACTER	ISTICS						
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 \text{ V}, T_{J} = 25^{\circ}\text{C}$			0.8	1.2	V
		I _S = 200 mA			0.7		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 5. Pulse Test: pulse width \leq 300 μ s, duty cycle \leq 2%

Surface-mounted on FR4 board using 1 sq in pad size with 1 oz Cu.
 Surface-mounted on FR4 board using 0.08 sq in pad size with 1 oz Cu.

^{6.} Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

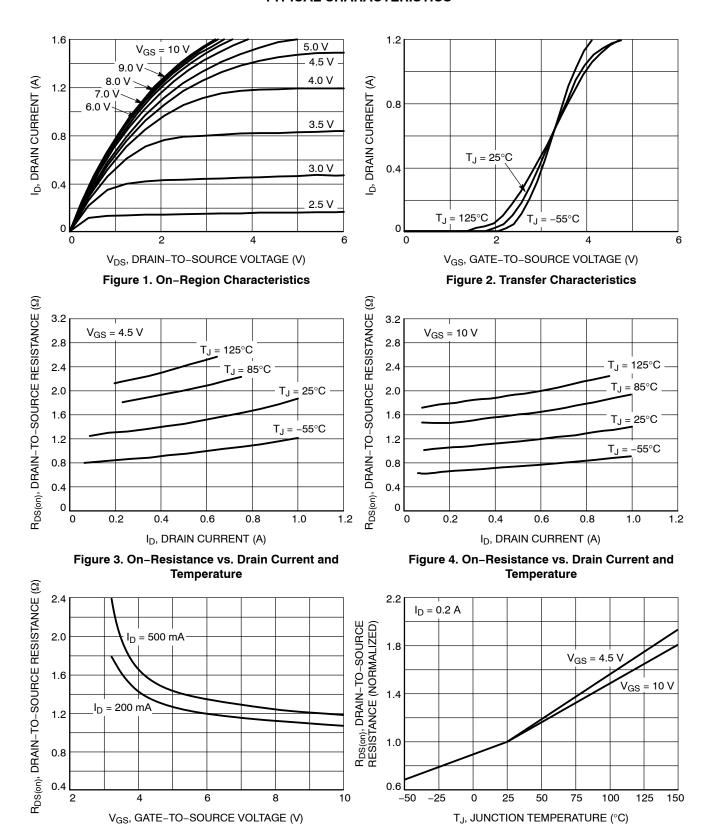


Figure 6. On-Resistance Variation with

Temperature

Figure 5. On-Resistance vs. Gate-to-Source

Voltage

TYPICAL CHARACTERISTICS

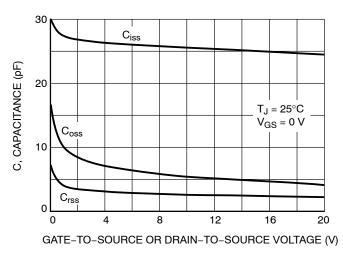


Figure 7. Capacitance Variation

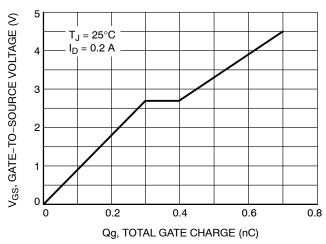


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

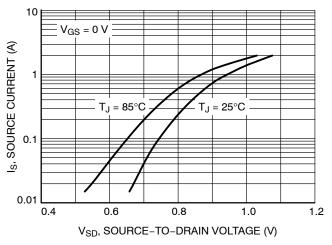


Figure 9. Diode Forward Voltage vs. Current

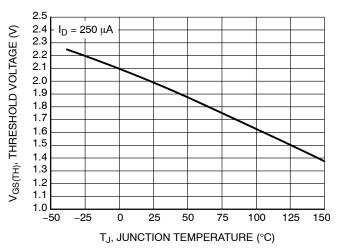


Figure 10. Threshold Voltage with Temperature

TYPICAL CHARACTERISTICS

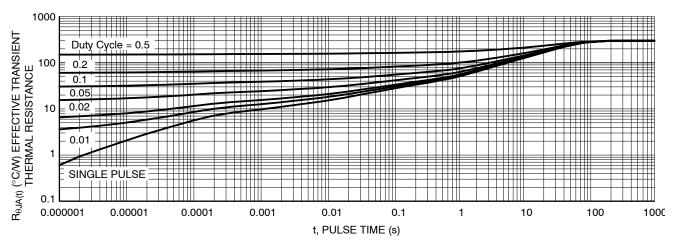


Figure 11. Thermal Response - 1 sq in pad

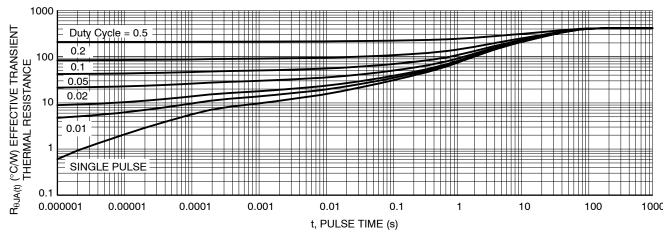


Figure 12. Thermal Response - minimum pad

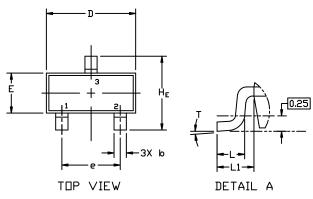


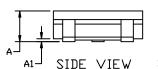


SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023









NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES			
DIM	MIN.	N□M.	MAX.	MIN.	N□M.	MAX.
Α	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
С	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
Ε	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
Т	0*		10°	0*		10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

STYLES ON PAGE 2

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^{*}This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23 (TO-236) CASE 318 ISSUE AT

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STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE	1	
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: N PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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