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EMC Tests and PCB Guidelines for Automotive Linear Regulators

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APPLICATION NOTE

Introduction

Electromagnetic compatibility (EMC) is important for the functionality and security of electronic devices. Today's designers must deal with steadily increasing system frequencies, changing power limits, high-density layouts required by more complex systems, and the ever-present need for low manufacturing cost. Therefore, it is necessary to optimize EMC.

Linear regulators supply several types of loads including microcontrollers, one of the key devices in automotive applications.

This document concentrates on EMC for automotive basic knowledge, test methods at the IC level and ON Semiconductor standards. PCB guide lines are included to prevent any board effect or external coupling.

Definition of EMC

Electromagnetic compatibility (EMC) is the capacity of a piece of equipment to work properly in its normal environment, and not create electrical disturbances that would interfere with other equipment.

Electromagnetic susceptibility (EMS) is the level of resistance to electrical disturbances such as electromagnetic fields and conducted electrical noise.

Electromagnetic interference (EMI) is the level of conducted/radiated electrical noise created by the equipment.

Standards are addressing EMS or EMI issues for every type of application area. These standards apply to finished equipment.

EMC tests must be performed on the sub-systems in order to evaluate and optimize applications for EMC performances. Standards for IC-level EMC testing have existed since 2003. Two Standards are commonly used: *IEC62132−4 (Direct Power Injection or DPI)* for EMS and the *IEC61967−4 (1 Ω/150 Ω method)*

Definition of Noise

Susceptibility to radio frequency interference is becoming a major concern for integrated circuits, with the propagation of new and powerful electromagnetic sources. Electrostatic discharges, mains transients, switching of high currents and voltages or radio frequency (RF) generators are just some of the causes of electromagnetic interference. EMI can be transferred by electromagnetic waves, conduction, and inductive/capacitive coupling.

The Linear Regulators Architecture

The linear approach is often considered for low output noise generation.

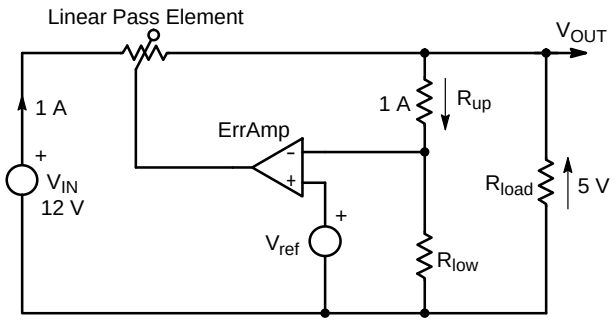


Figure 1. Linear Power Supply

However, efficiency is one of the limitations of the linear approach.

Intrinsically, linear regulators do not generate noise and EMC disturbances, but they can be susceptible to noise generated by other components like microcontrollers, SMPS, and logic circuits.

According to the IEC standards, Linear regulators are tested using the Direct Power Injection method (IEC62132−4).

Direct Power Injection

The RF disturbance (a sinusoidal waveform from 150 kHz to 1 GHz CW (Continuous Wave)) or AM (Amplitude Modulation, 1 kHz, 80%) is injected on the component pin under test through a decoupling block as shown on Figure 2. The DC block is realized by a capacitor. The RF disturbance is monitored through the directional coupler by measuring the forward power and the reflected power.

The continuous wave means the successive oscillations are identical under steady state conditions. The amplitude modulation (AM) is the process by which a continuous high frequency wave is caused to vary in amplitude by the action of another wave containing information.

The basic requirement when an amplitude modulation is applied is the peak power shall have the same value as the peak power when a continuous wave is applied, regardless the modulation index m.

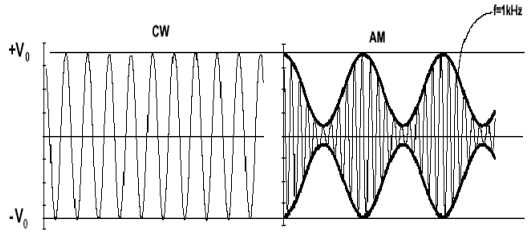
$$P_{AM-Peak} = P_{CW-Peak}$$

and

$$P_{AM} = P_{CW}\frac{2 + m^2}{2(1 + m)^2}$$

For example, 80% Amplitude Modulation, 1 kHz (m = 0.8) result is

$$P_{AM} = 0.407 \cdot P_{CW}$$



The forward power is the amount of power that is sent from the RF source towards the DUT without considering the RF power that is being reflected backwards by the DUT.

To reduce the reflection effects, the set up is built with 50 Ω cable and 50 Ω adapted printed circuit board tracks, so that the injection path is 50 Ω almost all the way from the RF generator to the DUT. However, the DUT impedance is strongly dependant on frequency, therefore creating reflections and resonant effects. An attenuator (3 dB) is inserted just before the capacitor to avoid errors due to cable effects.

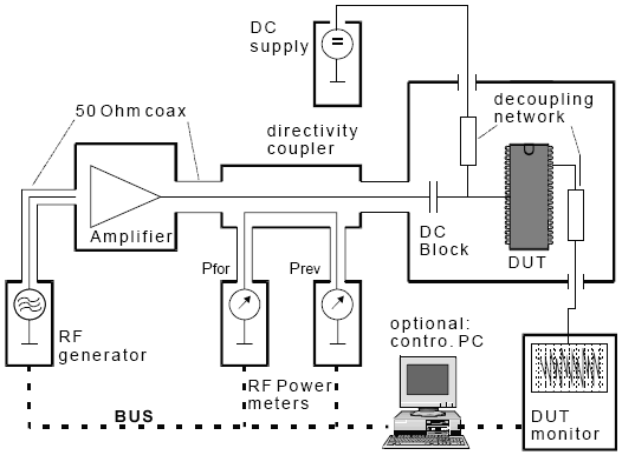


Figure 2. DPI Set Up

The following algorithm is used to test components with the DPI method.

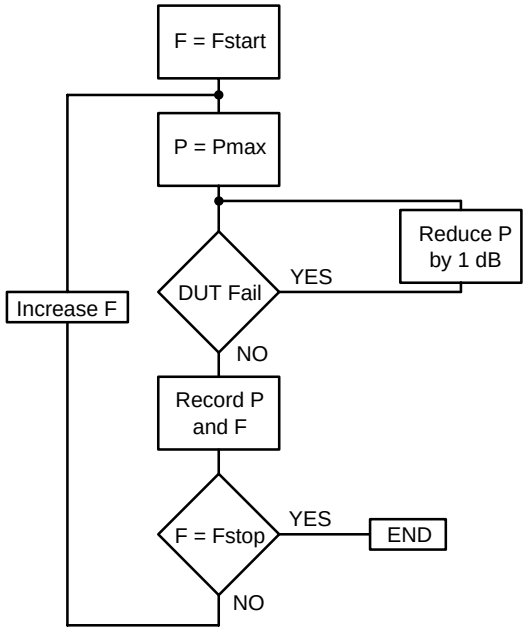


Figure 3. DPI Flowchart

For each frequency step, power is set to the specified power limit. If the device fails, the power is decreased in 1 dBm steps until the DUT exhibits correct performance.

Linear Regulators Tested with DPI Method

The usual limit is 1 W (30 dBm, Forward power CW) for global pins and 17 dBm, Forward power CW for local pins. A global pin carries a signal or power which enters or leaves the application board. A local pin carries a signal or power which does not leave the application board. It remains on the application board as a signal between two components. For linear regulators, the Input and Output pins are considered as global pins and are tested at the 30 dBm compliance limit. Some linear regulators have added features, such as Reset and Delay circuitry. In this case, associated pins are considered as local pins and tested to the 17 dBm compliance limit.

The usual failure condition is the Output voltage. For linear regulators with additional features, other pins are monitored and must maintain their correct state (logic pins).

Method: DPI according to IEC 62132-4

Frequency range: 1MHz to 1GHz

Frequency increment: 5%

Increment duration: 1 s

Frequency modulation: None (continuous wave)

RF Calibration method: Substitution

Power compliance limit: 33dBm for global pin
17dBm for local pin

Power step size: 1dBm

Device pins injected: VIN; RESET, VOUT

Device pins monitored: VOUT; RESET

Load resistance: 100 ohms

DC input voltage: 12V

Acceptance criteria:
Output voltage within 4% of nominal value
Digital outputs remain in correct state +-1V

Figure 4. Typical Test Conditions

General Golden Rules for PCB

All components should be placed with an appropriate functional group and their tracks routed within their designated PCB area. A recommended arrangement of functional groups on PCB is shown in Figure 8.

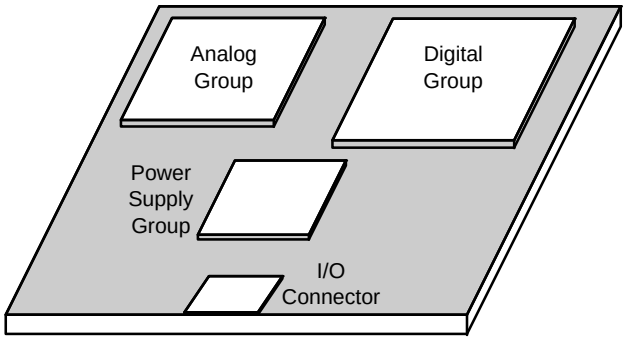


Figure 5. Arrangement of Functional Groups on PCB

Place ground plane(s) under all components and all their associated tracks. A continuous ground plane with no avoidance is recommended.

- A Good Ground Plane is Achieved by Using a Complete Layer for Ground
- Do Not Cut the Ground Plane by Routing Signal Lines in GND Plane
- Provide a Length/Width Ratio less than 5 for the PCB (At a Ratio > 5 the Inductance of the Ground Plane Increases)

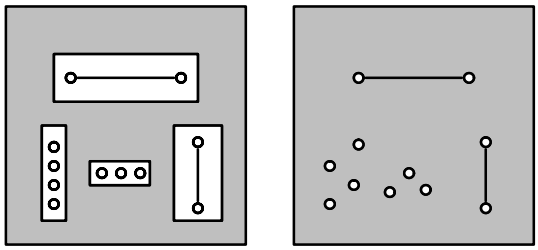


Figure 6. Maximizing Ground on PCB

Connection to Ground

- Connect Each Component Directly to Plane
- Use a via for Each Component-Pin for GND-Connection Instead of GND-Traces
- Connections to Ground must be Shorter than 0.5 mm (20 mils)

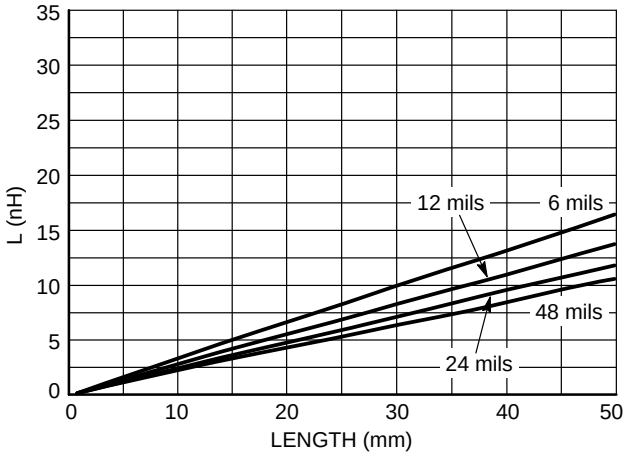


Figure 7. Inductance and Capacitance Values of a Strip Line Above a Ground Plane

Trace widths should be around 20 mils to reduce partial parasitic inductance.

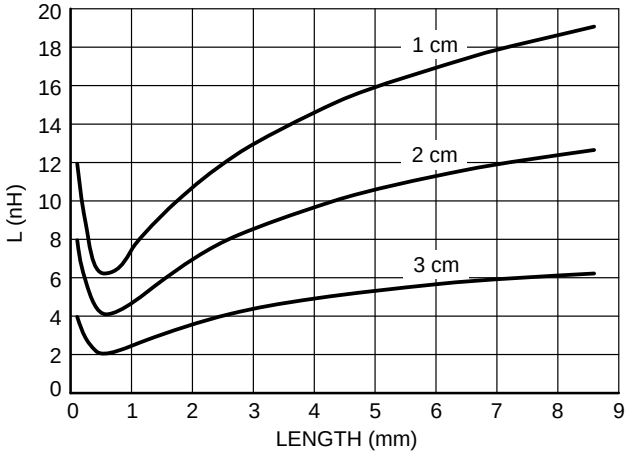


Figure 8. Effect of the Trace's Width on Parasitic Inductance

Particular Linear Regulator Guidelines

Power supplies should be located as close to the power entry point to the PCB, and as close as possible to powered circuitry. Closely routed tracks (to minimize the area between conductors, and hence the inductance) should be used to connect the power source to the local power distribution system.

Power feeds should always be decoupled at their entry points onto the PCB.

Bulk capacitors should always be parallel decoupled with one or more lower valued high frequency capacitors with low ESL (equivalent series inductance). Place the smallest value decoupling capacitor closest to a device to be decoupled.

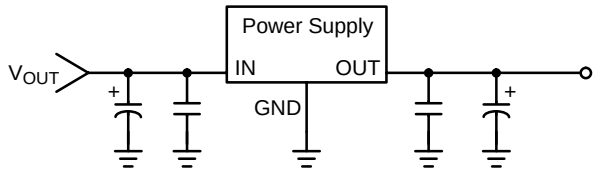


Figure 9. Power System

High-frequency, low-inductance ceramic capacitors should be used for IC decoupling at each power pin. Use 0.1 μF for up to 15 MHz, and 0.01 μF over 15 MHz. The decoupling capacitor should be located as close as physically possible to the IC's power pin.

Printed circuit board traces which carry high switching current with fast rise/fall times (5−10 ns) should maintain at least 3 mm spacing from other signal traces which run parallel to them, and/or ground guard traces should be placed between them.

Corresponding power and ground signals should always be routed in parallel to minimize loop area thus reducing loop impedance (Figure 10).

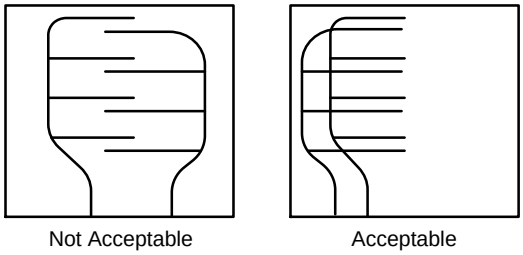


Figure 10. PS Routing

Layout Example

Two boards have been made. The first one follows the EMC design guidelines listed above. The second one is a typical applications board without consideration of EMC rules. A linear regulator with reset function has been tested with the DPI method.

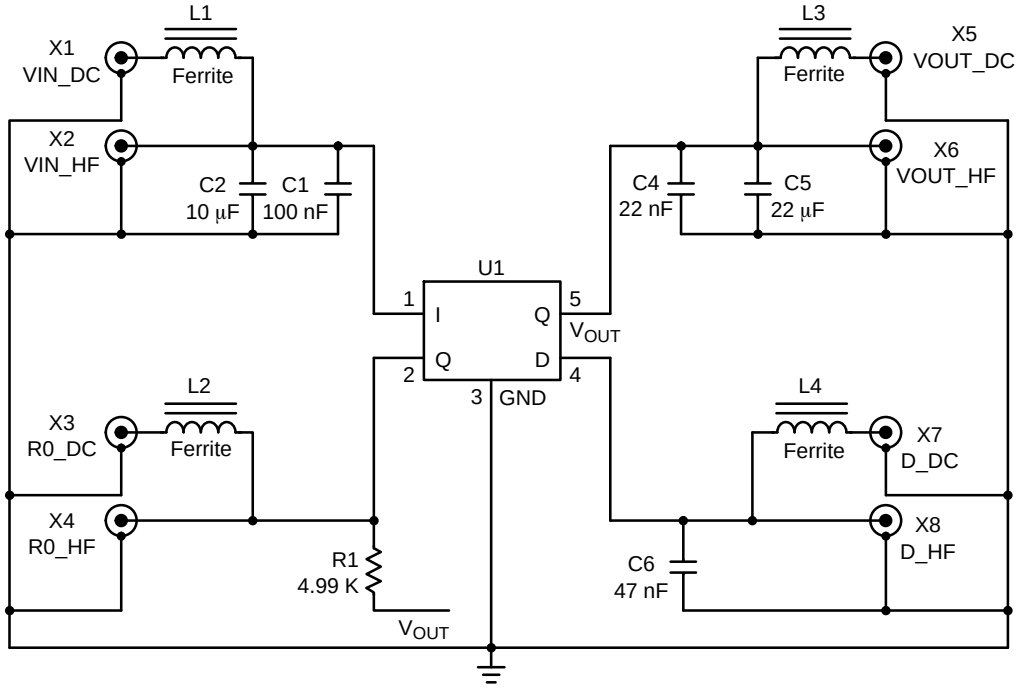


Figure 11. Board Schematic

The board schematic includes tantalum capacitors on the input and output. Two small ceramic capacitors have been added.

Figure 4 shows the failure criteria used for this example. 4% variation for the output voltage and 2 V for the reset considered as a logic output pin are considered acceptable.

Good EMC Test Board

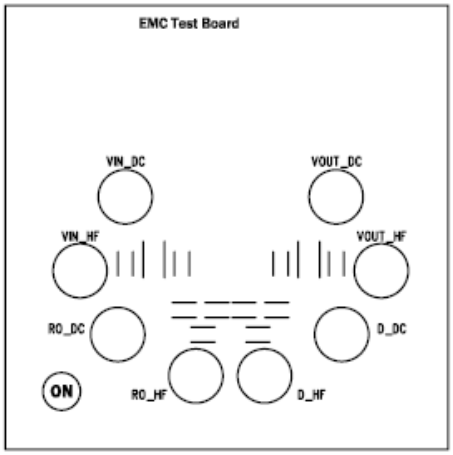


Figure 12. Assembly Top Good Layout

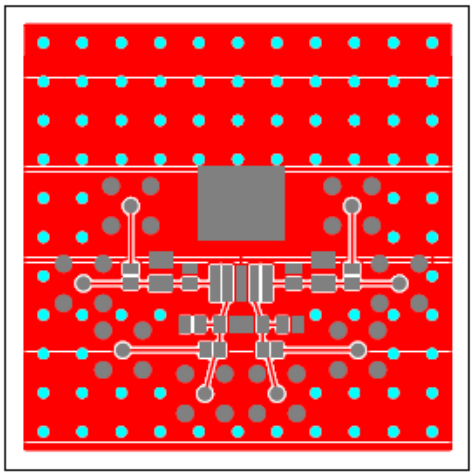


Figure 13. Top Layer EMC Layout

20 mils trace widths are used with short connections. Input and output capacitors are located as close as possible to the DUT pin. It is a four layer board with ground plane.

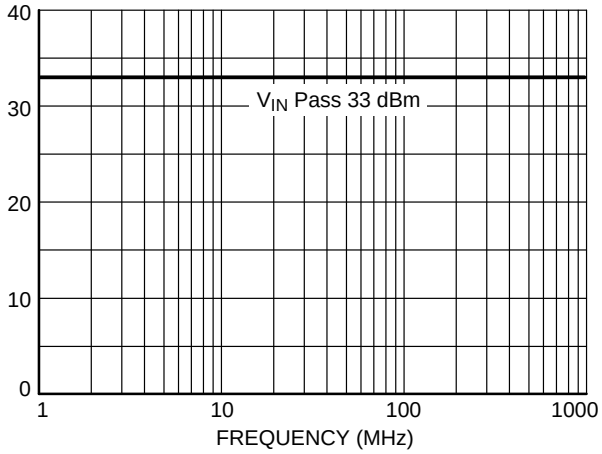


Figure 14. DPI on V_{IN} Pin

The Device passes 33 dBm injection on V_{IN} pin with Reset and V_{OUT} pins monitored.

PCB Without Consideration of EMC Rules

The second PCB is a demo board. The same components are used with a different layout.

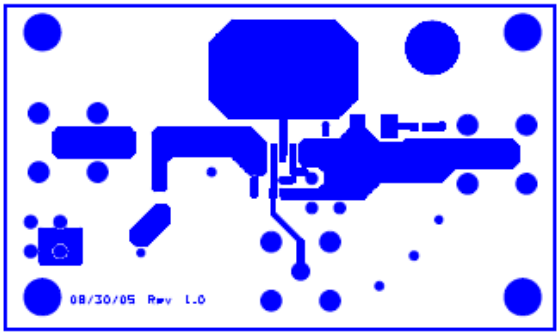


Figure 15. Top Layer Typ Layout

The demo board is a two layer board with ground plane. The trace widths are bigger than 20 mils which increases parasitic inductance. The distance from capacitor to the DUT pins is more than 1 cm. The layout does not follow the power supply guide lines.

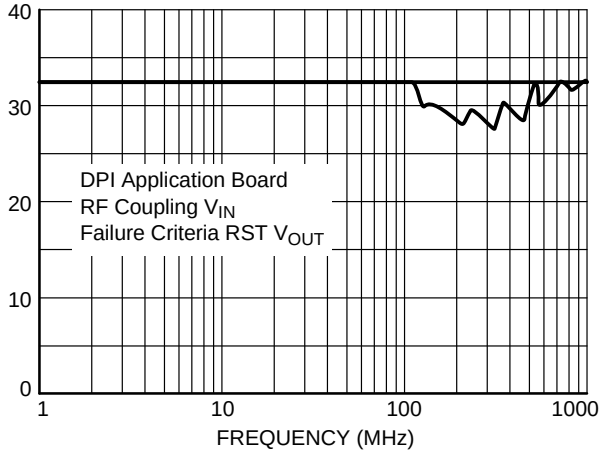


Figure 16. DPI on V_{IN} Pin

In the same test condition, the device is not compliant with 33 dBm power limit in the whole frequency range. Issues appear between 100 MHz and 1 GHz. The lower limit is around 25 dBm @ 205 MHz The RF signal perturbed the output signal and created a reset.

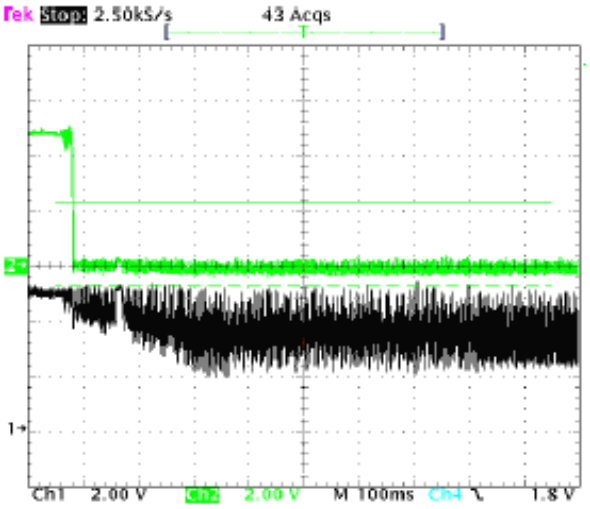


Figure 17. V_{OUT} and Reset Errors

33 dBm is 2 W injection; 25 dBm is 0.3 W injection which is a large performance difference for the same bill of materials.

Conclusion

As started in the introduction, EMC takes into account Susceptibility and Emission of the components. Due to the PCB connections, the coupling paths have to be considered such as another way for EMC improvement at system level.

Obviously, EMI must reach the traces in order to disturb the components. This means that the loops, long length and large surface of the conductors are vulnerable to EMI, making the PCB the principal subject of EMC improvements.

Following EMC rules will reduce design costs and time-to-market, while improving reliability and performance of the design.

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[5] M Montrose, *"Printed Circuit Board Design Techniques for EMC Compliance"*, 1996 IEEE Press

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