Dual Self-Protected Low Side Driver with Temperature and Current Limit

NCV8406DD

V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D TYP (Limited)
65 V	210 mΩ	7.0 A

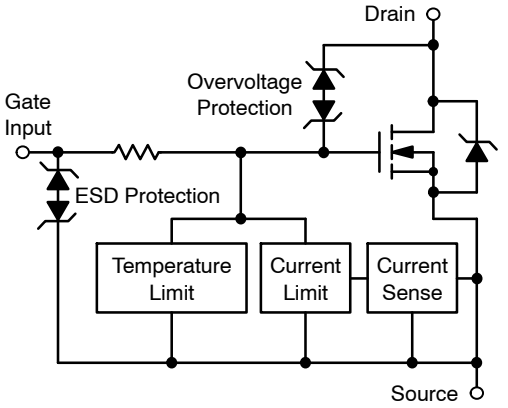
NCV8406DD is a dual protected Low−Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain−to−Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- These Devices are Faster than the Rest of the NCV Devices
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

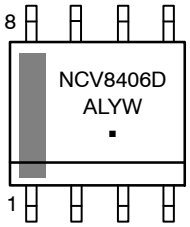
Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial



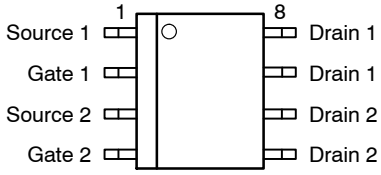
MARKING DIAGRAM

SO−8
CASE 751



NCV8406D = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	60	Vdc
Gate−to−Source Voltage	V_{GS}	±14	Vdc
Drain Current Continuous	I_D	Internally Limited	
Power Dissipation per Channel, both channels loaded equally @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 0.57 0.78	W
Total Power Dissipation, only one channel loaded @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 0.93 1.2	W
Thermal Resistance, both channels loaded equally Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2) Junction−to−Case (Soldering Point)	 $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	 107.8 79.4 29	°C/W
Thermal Resistance, only one channel loaded Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2) Junction−to−Case (Soldering Point)	 $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	 133.6 103.8 29	°C/W
Single Pulse Inductive Load Switching Energy (Starting T_J = 25°C, V_{DD} = 50 Vdc, V_{GS} = 5.0 Vdc, I_L = 2.1 Apk, L = 50 mH, R_G = 25 Ω)	E_{AS}	110	mJ
Load Dump Voltage (V_{GS} = 0 and 10 V, R_I = 2 Ω, R_L = 7 Ω, t_d = 400 ms)	V_{LD}	75	V
Operating Junction Temperature Range	T_J	−40 to 150	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted onto a 80 x 80 x 1.6 mm single layer FR4 board (100 sq mm, 1 oz. Cu, steady state.
2. Mounted onto a 80 x 80 x 1.6 mm single layer FR4 board (645 sq mm, 1 oz. Cu, steady state.

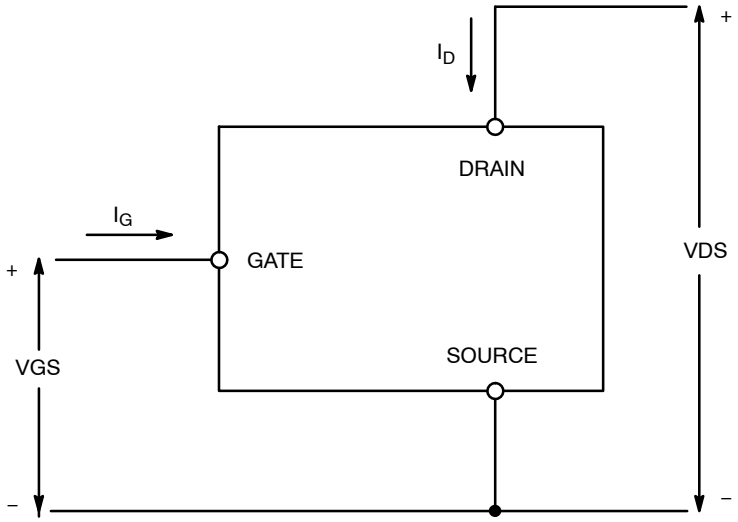


Figure 1. Voltage and Current Convention

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Clamped Breakdown Voltage	(V_{GS} = 0 V, I_D = 2 mA)	$V_{(BR)DSS}$	60	65	70	V
Zero Gate Voltage Drain Current	(V_{DS} = 52 V, V_{GS} = 0 V)	I_{DSS}	–	22	100	μA
Gate Input Current	(V_{GS} = 5.0 V, V_{DS} = 0 V)	I_{GSS}	–	30	100	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	(V_{DS} = V_{GS}, I_D = 150 μA) Threshold Temperature Coefficient	$V_{GS(th)}$	1.2 –	1.66 4.0	2.0 –	V −mV/°C
Static Drain−to−Source On−Resistance (Note 3)	(V_{GS} = 10 V, I_D = 2.0 A, T_J @ 25°C)	$R_{DS(on)}$	–	185	210	mΩ
Static Drain−to−Source On−Resistance (Note 3)	(V_{GS} = 5.0 V, I_D = 2.0 A, T_J @ 25°C) (V_{GS} = 5.0 V, I_D = 2.0 A, T_J @ 150°C)	$R_{DS(on)}$	– –	210 445	240 520	mΩ
Source−Drain Forward On Voltage	(I_S = 7.0 A, V_{GS} = 0 V)	V_{SD}	–	0.9	1.1	V
SWITCHING CHARACTERISTICS (Note 6)						
Turn−on Delay Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 10% V_{in} to 10% I_D	$td_{(on)}$	–	127	–	ns
Turn−on Rise Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 10% I_D to 90% I_D	t_{rise}	–	486	–	ns
Turn−off Delay Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 90% V_{in} to 90% I_D	$td_{(off)}$	–	1600	–	ns
Turn−off Fall Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 90% I_D to 10% I_D	t_{fall}	–	692	–	ns
Slew Rate ON	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 70% to 50% V_{DD}	dV_{DS}/dT_{on}	–	79	–	V/μs
Slew Rate OFF	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 50% to 70% V_{DD}	dV_{DS}/dT_{off}	–	27	–	V/μs
SELF PROTECTION CHARACTERISTICS (Note 4)						
Current Limit	V_{DS} = 10 V, V_{GS} = 5.0 V, T_J = 25°C (Notes 5, 7) V_{DS} = 10 V, V_{GS} = 5.0 V, T_J = 150°C (Notes 5, 6, 7) V_{DS} = 10 V, V_{GS} = 10 V, T_J = 25°C (Notes 5, 7)	I_{LIM}	5.0 3.5 6.5	7.0 4.5 8.5	9.5 6.0 10.5	A
Temperature Limit (Turn−off)	V_{GS} = 5.0 V (Notes 6, 7)	$T_{LIM(off)}$	150	180	200	°C
Thermal Hysteresis	V_{GS} = 5.0 V	$\Delta T_{LIM(on)}$	–	10	–	°C
Temperature Limit (Turn−off)	V_{GS} = 10 V (Notes 6, 7)	$T_{LIM(off)}$	150	180	200	°C
Thermal Hysteresis	V_{GS} = 10 V	$\Delta T_{LIM(on)}$	–	20	–	°C
Input Current during Thermal Fault	V_{DS} = 0 V, V_{GS} = 5.0 V, T_J = T_J > $T_{(fault)}$ (Note 6) V_{DS} = 0 V, V_{GS} = 10 V, T_J = T_J > $T_{(fault)}$ (Note 6)	$I_{g(fault)}$	– –	5.9 12.3	–	mA
ESD ELECTRICAL CHARACTERISTICS						
Electro−Static Discharge Capability Human Body Model (HBM) Machine Model (MM)		ESD	 6000 500	 – –	 – –	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Current limit measured at 380 μs after gate pulse.
6. Not subject to production test.
7. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

TYPICAL PERFORMANCE CURVES

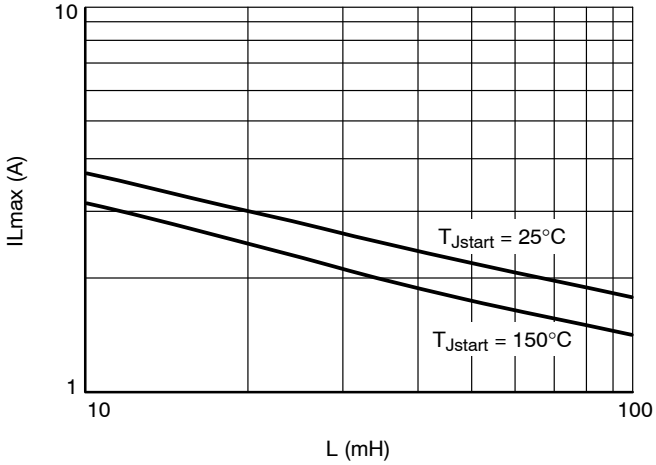


Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance

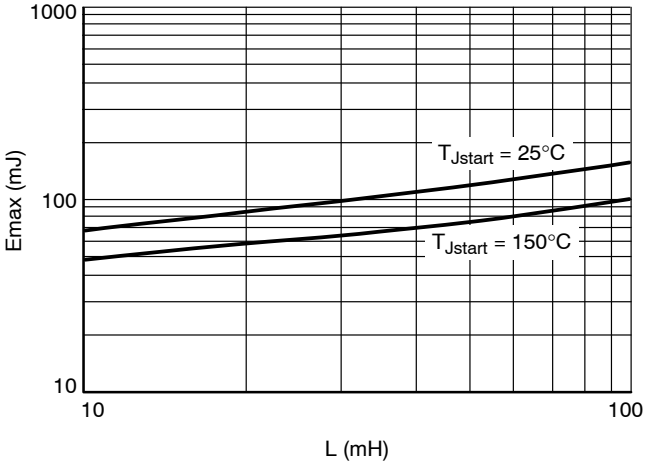


Figure 3. Single−Pulse Maximum Switching Energy vs. Load Inductance

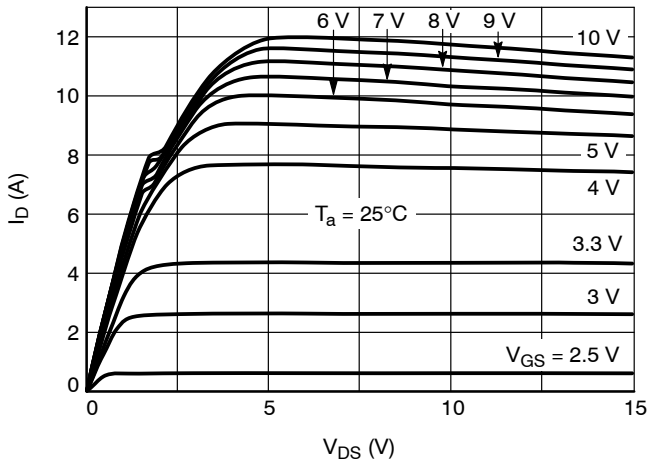


Figure 4. On−state Output Characteristics

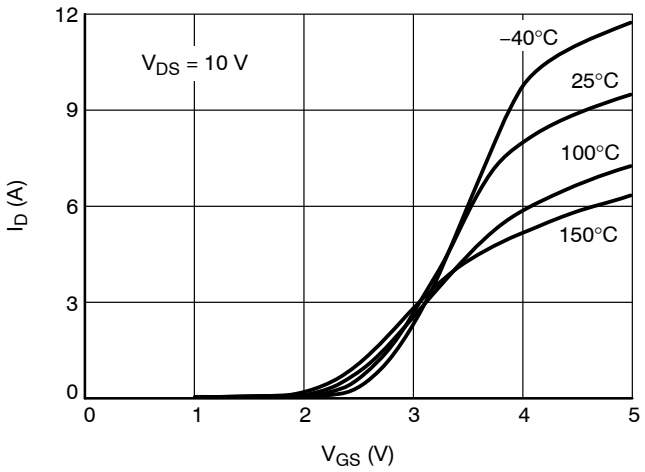


Figure 5. Transfer Characteristics

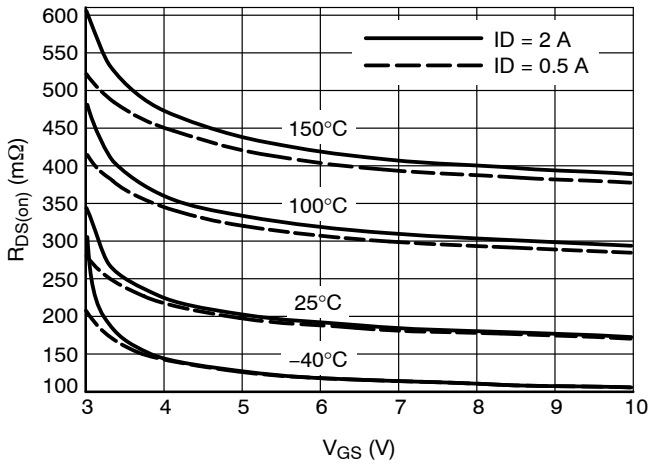


Figure 6. $R_{DS(on)}$ vs. Gate−Source Voltage

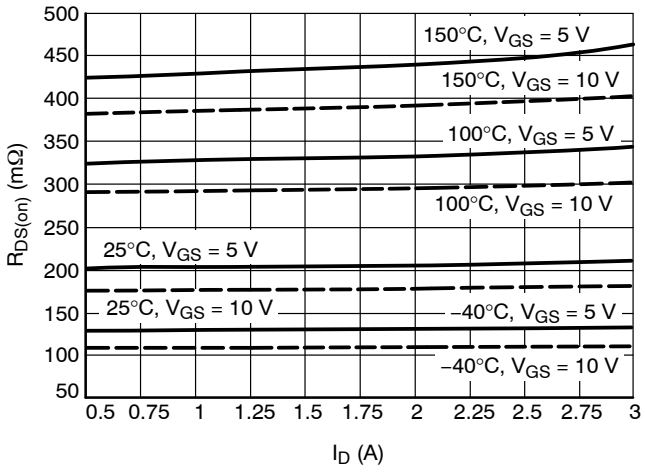


Figure 7. $R_{DS(on)}$ vs. Drain Current

TYPICAL PERFORMANCE CURVES

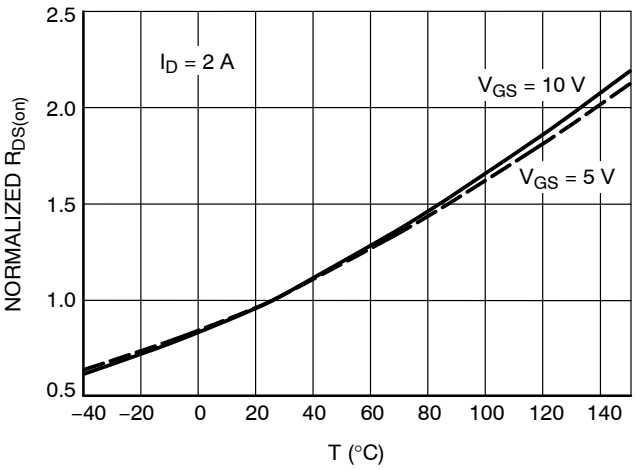


Figure 8. Normalized $R_{DS(on)}$ vs. Temperature

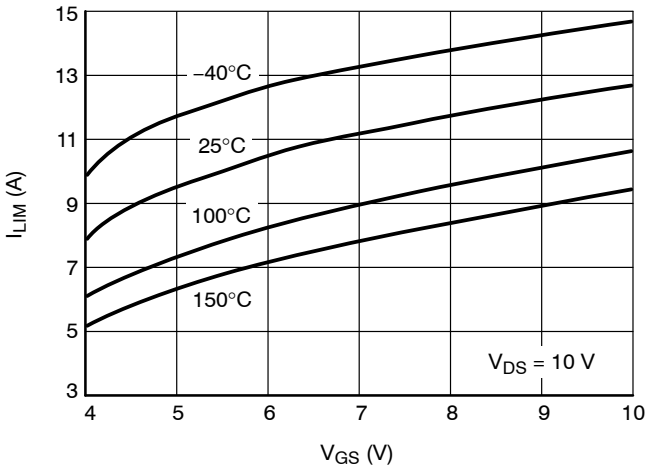


Figure 9. Current Limit vs. Gate−Source Voltage

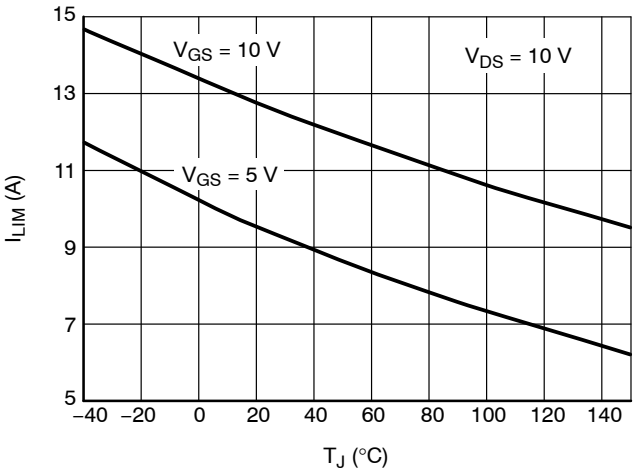


Figure 10. Current Limit vs. Junction Temperature

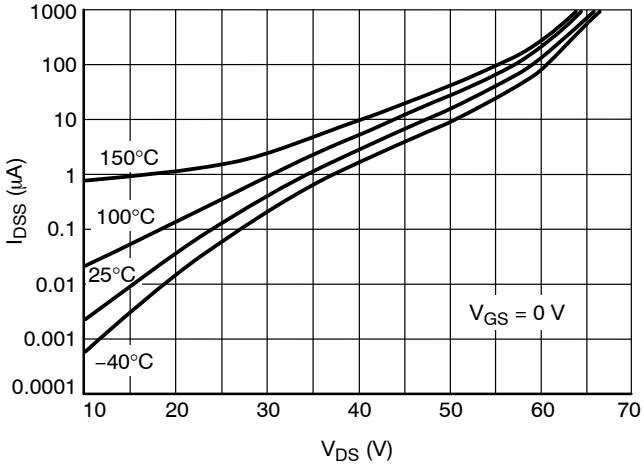


Figure 11. Drain−to−Source Leakage Current

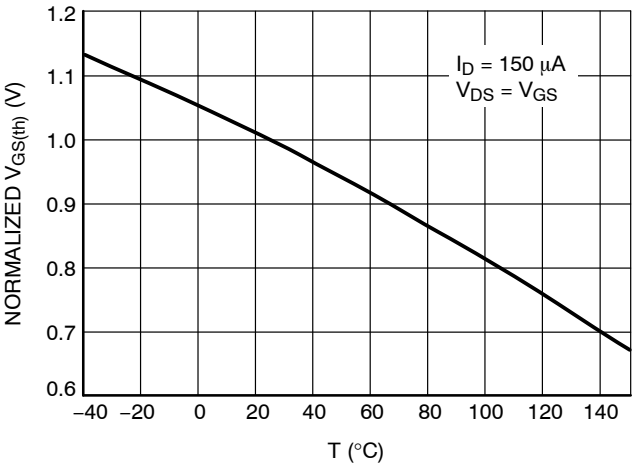


Figure 12. Normalized Threshold Voltage vs. Temperature

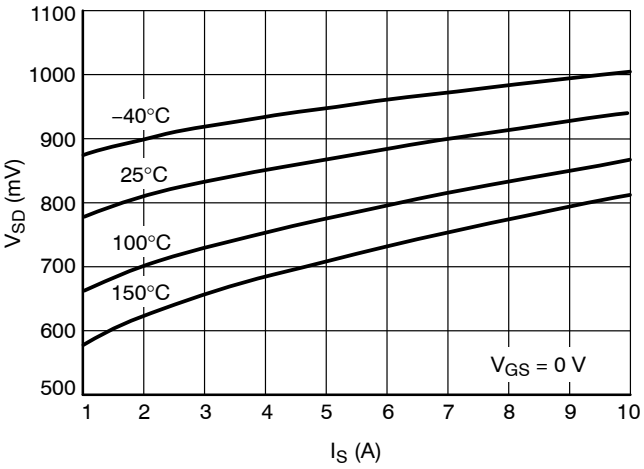


Figure 13. Source−Drain Diode Forward Characteristics

TYPICAL PERFORMANCE CURVES

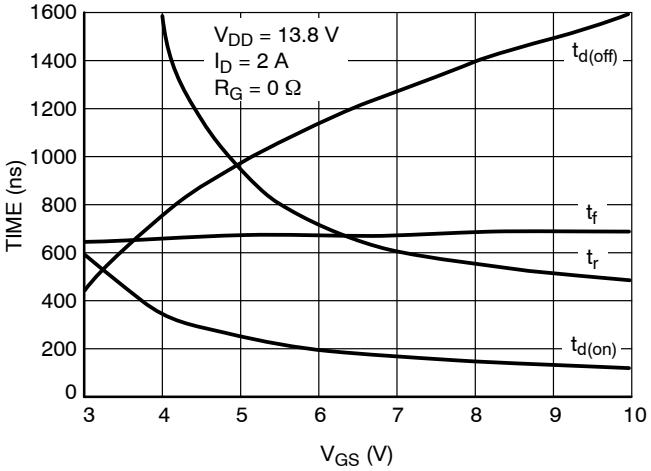


Figure 14. Resistive Load Switching Time vs. Gate−Source Voltage

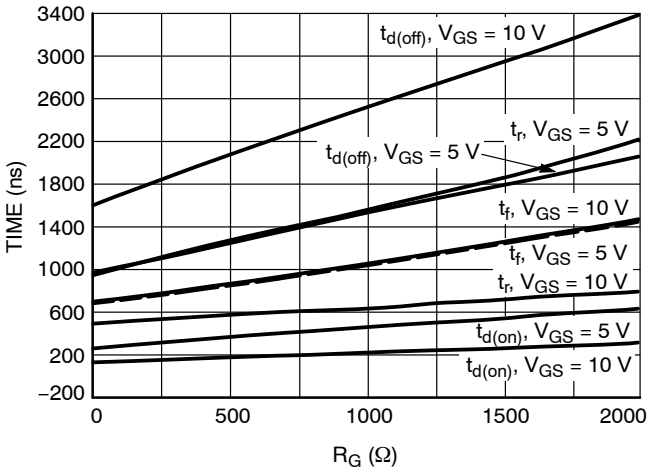


Figure 15. Resistive Load Switching Time vs. Gate Resistance

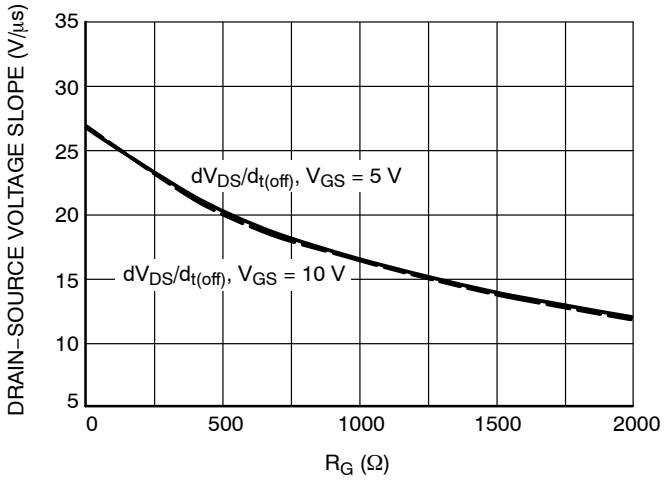


Figure 16. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

TYPICAL PERFORMANCE CURVES

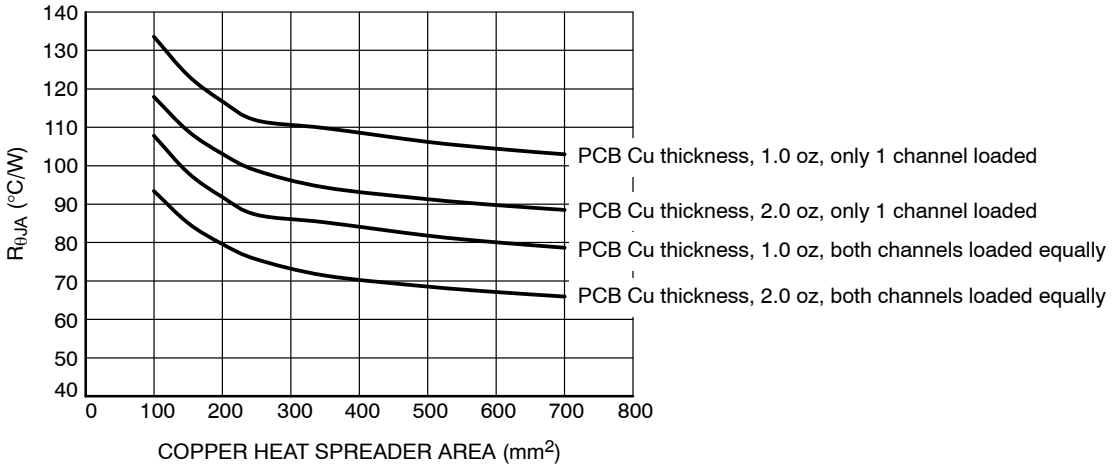


Figure 17. $R_{\theta JA}$ vs. Copper Area

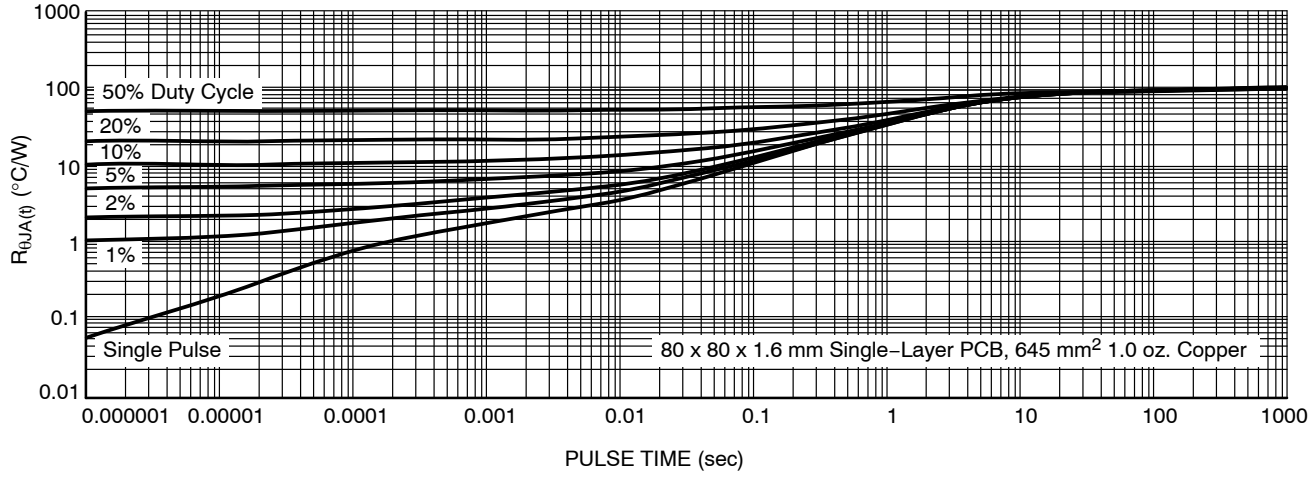


Figure 18. Transient Thermal Resistance, Only 1 Channel Loaded

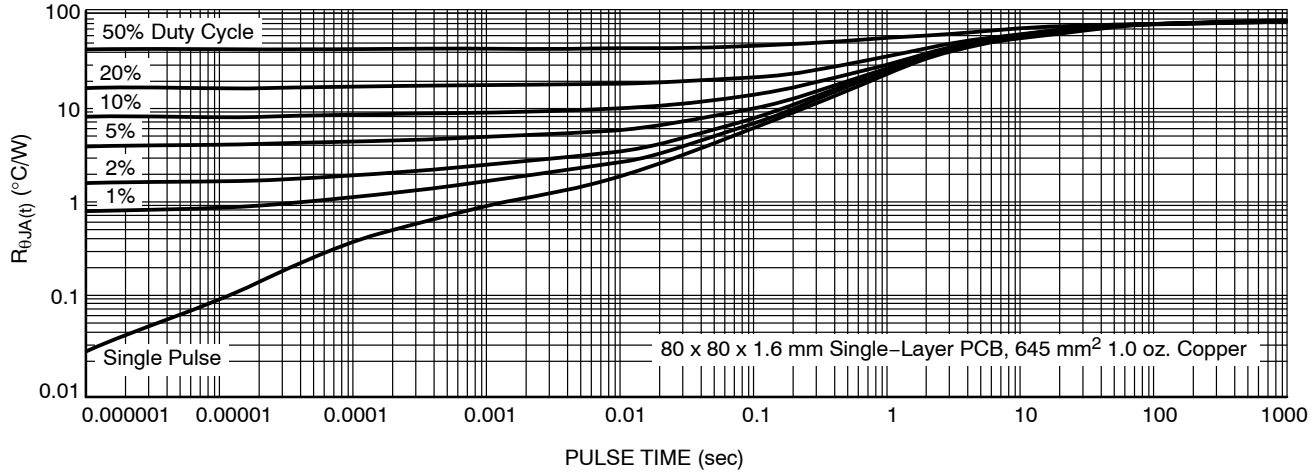


Figure 19. Transient Thermal Resistance, 2 Channels Loaded

TEST CIRCUITS AND WAVEFORMS

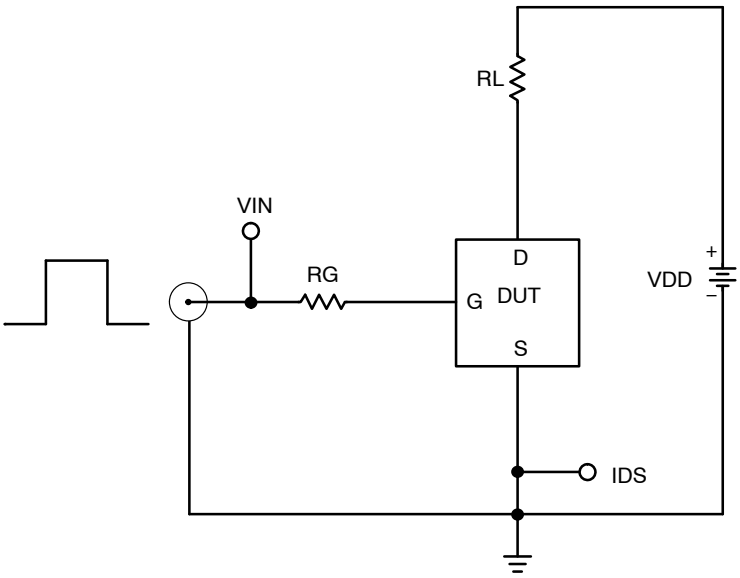


Figure 20. Resistive Load Switching Test Circuit

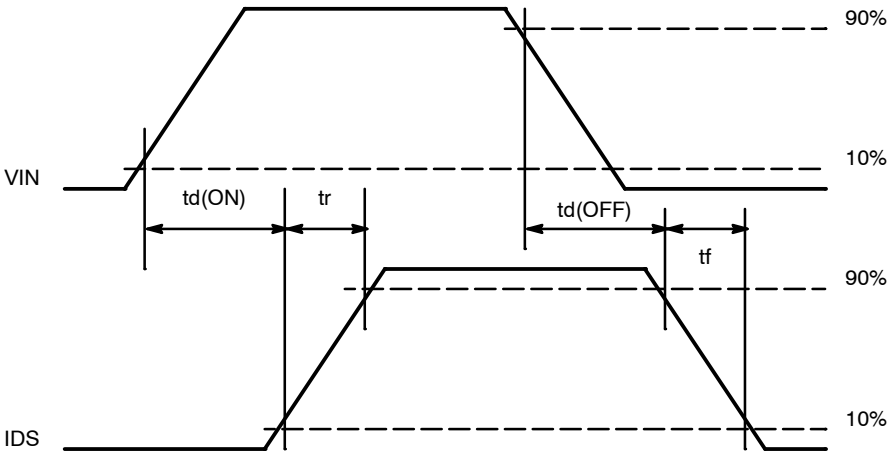


Figure 21. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

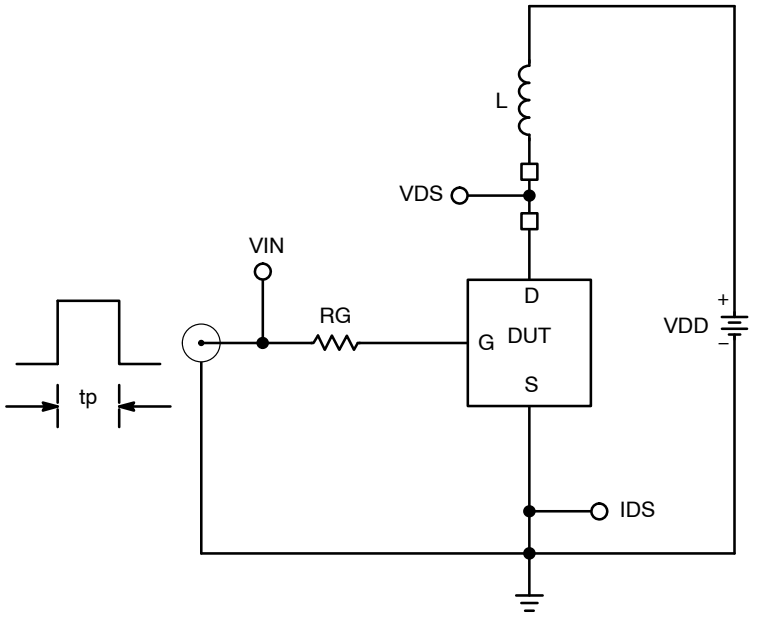


Figure 22. Inductive Load Switching Test Circuit

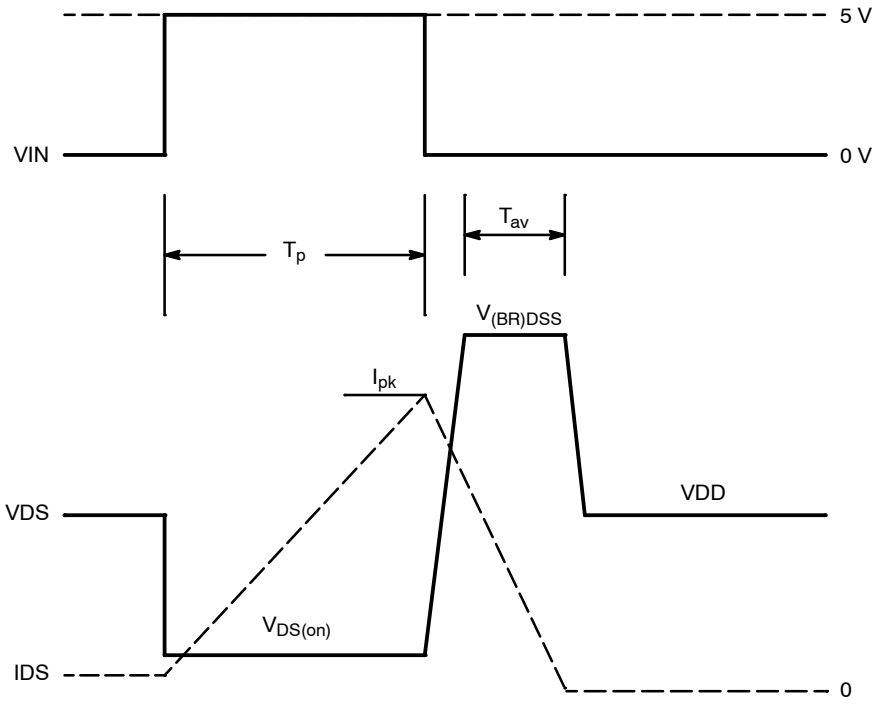


Figure 23. Inductive Load Switching Waveforms

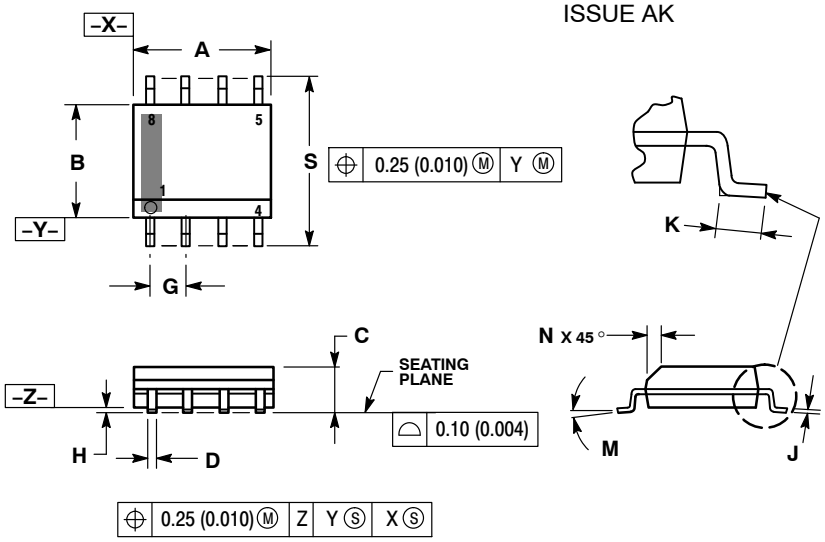
ORDERING INFORMATION

Device	Package	Shipping†
NCV8406DD1CR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

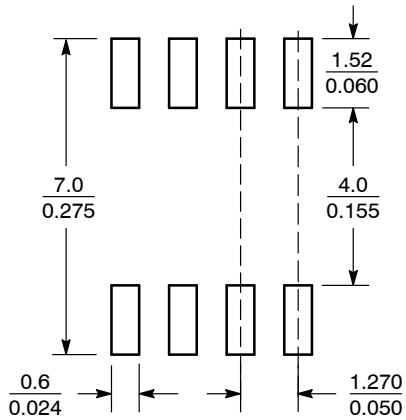
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales